

A New H-Bridge Hybrid Modular Converter (HBHMC) for HVDC Application: Operating Modes, Control and Voltage Balancing

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Abstract - An H-bridge hybrid modular converter (HBHMC) is proposed for HVDC applications. It uses a wave-shaping circuit (WSC) consisting of series-connected full-bridge submodules (FBSMs) at the output of the main H-bridge converter (MHBC). For a three-phase system, three HBHMCs are connected either in series (series-HBHMC) or in parallel (parallel-HBHMC) across the dc-link. The operating modes of HBHMC, novel modulation strategies for voltage balancing of FBSMs, and control of HBHMC based HVDC system are presented in this paper. A detailed comparison between HBHMC and other hybrid topologies is performed on the basis of required number of switches and capacitors. The HBHMC has the features of dc fault blocking capability, lower footprint structure and extra degree of freedom for submodules capacitor voltage balancing. The efficacy of the HBHMC based HVDC system for three-phase balanced and unbalanced grid conditions and its fault tolerant capability are validated using PSCAD simulation studies. Further, the feasibility of proposed converter under normal, and dc fault conditions, and of the proposed capacitor voltage control scheme are validated experimentally by using a three-phase grid connected HBHMC laboratory prototype. The results demonstrate the effectiveness of the proposed HBHMC topology, control techniques, and satisfactory responses of the HBHMC based HVDC system.

Index Terms-- dc fault tolerant, H-bridge hybrid modular converter (HBHMC), HVDC systems, and modular multilevel converter.

NOMENCLATURE

MMC	Modular multilevel converter
VSC	Voltage source converter
HVDC	High voltage direct current
SM	Submodule
HBSM	Half bridge submodule
FBSM	Full bridge submodule
HBHMC	H-bridge hybrid modular converter
MHBC	Main H-bridge circuit
HMC	Hybrid multilevel converter
WSC	Wave shaping circuit
DSs	Director switches
HCMC	Hybrid cascaded multilevel converter
AAMMC	Alternate arm modular multilevel converter
CTFB-HMC	Controlled transition full bridge hybrid multilevel converter
FACTS	Flexible ac transmission system
HCI	Half cycle isolation
AZCI	Across zero crossing isolation
IGBT	Insulated-gate bipolar transistor
PDPWM	Phase disposition pulse width modulation

I. INTRODUCTION

MODULAR multilevel converter is fast becoming one of the most preferred topologies for VSC based HVDC transmission systems [1]-[4]. This is primarily due to its advantages like modularity, scalability, low conduction losses, low harmonic filter requirement, and low dv/dt , which allows

the use of transformer with low insulation requirement. However, MMC has limitations such as, the requirement of a large number of devices and capacitors, inability to block/limit fault current in the event of a dc side fault without using a dc circuit breaker, and the presence of circulating currents in each phase-leg of the MMC [5]-[10]. The circulating current has a significant impact on the ratings of the converter components, capacitors voltage ripples and power losses. A circulating current control is necessary to reduce such impacts [11]-[13]. Moreover, during a dc side fault, a high fault current flows through freewheeling diodes connected across each IGBTs in the MMC [5]-[17]. One of the approaches to tackle this problem is to use a dc circuit breaker as recently proposed in [14]-[17]. In the second approach, instead of the HBSM, another SM with the capability to produce the opposite polarity voltage is used that blocks/limits the fault current magnitude in case of dc side fault [18]-[22]. In the third approach, the converter configuration itself is modified and by using the FBSMs, the fault current limitation is achieved. This family of converters is called as the HMCs [23]-[34]. HMCs consist of mainly two parts, a DS and a WSC. DSs are the series connection of semiconductor switches and WSC is formed by connecting stacks of FBSMs in series.

Among the HMCs, the HCMC has dc fault tolerant capability, lower number of SMs in WSC and quarter the number of SM capacitors to that in MMC, which leads to smaller footprint and lower losses [23]-[26], [30]. However, it has higher losses in the DSs because of hard switching and it requires low order harmonic filters to mitigate low energy spikes due to mis-synchronization of DSs and WSC [24]. Moreover, for balancing of SMs capacitor voltages either more number of SMs are required or the DSs are required to switch at higher frequency, which leads to higher losses [24], [25], [31]. The AAMMC, proposed in [27]-[29], has features like, dc fault tolerant capability, half the number of SMs to that in the MMC and lower losses. However, for the smooth current commutation between upper and lower arms and for the capacitor voltage balancing in WSC, a short duration overlap period is required [31]. It creates a high inrush current in the arms and a suitably sized arm inductor is required for suppressing this inrush current. The parallel hybrid MMC is another promising topology for HVDC applications because of lower component count and soft switching of DSs [33], [34]. However, its main limitations are that it cannot block/limit dc fault current and it has lower order harmonics at the dc-link. Due to these harmonics the dc voltage cannot be regulated to a constant value, which compromises the power control [34]. Recently, another HMC is proposed which uses the WSC across the load [35]. The DSs of this topology are operated diagonally when the output voltage is clamped to dc-link voltage value, thus allowing the energy exchange between the dc-link and FBSMs. This time period is small and in case of high active power requirement the converter is required to take energy from

dc-link within that small period, which may cause high inrush current. Hence, it requires a dc side inductor and circulating device to limit the inrush current. Moreover, this converter does not have dc fault tolerant capability.

This paper proposes an H-bridge hybrid modular converter (HBHMC) topology, which addresses some of the issues of the existing HMC topologies as discussed above. The HBHMC topology has dc fault tolerant capability, small footprint structure, high dc-link utilization, an extra degree of freedom for SM capacitor voltage balancing, and it can be extended to high voltage-low current or low voltage-high current applications. In this paper, the single phase and three phase HBHMC structures, modes of operation of HBHMC, the WSC capacitor voltage balancing scheme by appropriately selecting powering and isolation modes, and individual capacitor voltage balancing scheme of WSC SMs of HBHMC are presented. The efficacy of the proposed voltage control schemes, modulation and control of HBHMC and dc fault tolerant capability of the converter are validated using both simulation and experimental studies. The detailed simulation studies of an HBHMC based HVDC system for various different operating conditions are carried out using PSCAD/EMTDC. The experimental studies are performed using a three-phase grid connected HBHMC hardware prototype. Furthermore, a comparative study is performed between the proposed and the other existing hybrid converter topologies.

II. H-BRIDGE HYBRID MODULAR CONVERTER

A. Single-phase configuration

The proposed single-phase HBHMC is shown in Fig. 1. Like other HMCs discussed in the previous section, this converter also has two main parts, a MHBC and WSC. The MHBC consists of four switches (DS_{x1} - DS_{x4}), which are series connection of fully controllable semiconductor switches to withstand high per phase dc-link voltage (V_{dcx}). These switches are operated at the fundamental frequency. The switches of MHBC directs the current either to the positive dc terminal, negative dc terminal, or it freewheels either through DS_{x1} and DS_{x2} or through DS_{x3} and DS_{x4} . To generate sinusoidal output voltage across the load, the WSC is used at the output of MHBC. The WSC is a series connection of FBSMs and these are switched at a higher frequency. The WSC is responsible for the multilevel converter output voltage waveform generation with very low distortion.

The output voltage states of the MHBC can be either $+V_{dcx}$, 0, or $-V_{dcx}$ as summarized in Table I. For simplicity only two FBSMs are considered to be connected in series with MHBC as shown in Fig. 1. If the voltage of each FBSM capacitor is regulated to $V_{dcx}/2$, five output voltage (V_x) levels ($+V_{dcx}$, $+V_{dcx}/2$, 0, $-V_{dcx}/2$, and $-V_{dcx}$) can be obtained. The different switching states for generating five voltage levels and the corresponding states of capacitor voltages are summarized in Table II. The symbols \uparrow , \downarrow , and \rightarrow indicate charging, discharging, and no change in capacitor voltage, respectively.

In Table II, the highlighted states are the additional switching states obtained compared to that in the HCMC topology presented in [25], [26]. These states give an extra degree of freedom for the capacitor voltage balancing of WSC in HBHMC. This is because, for the same direction of current and for a given voltage level output, the SM capacitors can be either charged or discharged in the desired manner. This degree of freedom is not present in the existing HCMC. Moreover, the

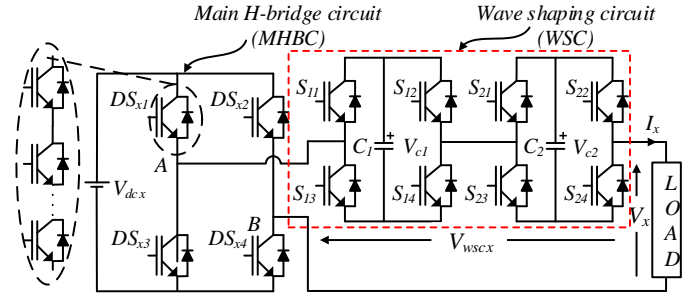


Fig. 1 Block diagram of single-phase HBHMC

TABLE I
SWITCHING STATES OF MHBC IN HBHMC

DS_{x1}	DS_{x2}	DS_{x3}	DS_{x4}	MHBC output voltage
1	0	0	1	$+V_{dcx}$
0	1	1	0	$-V_{dcx}$
0	0	1	1	0
1	1	0	0	0

TABLE II
SWITCHING SCHEME OF HBHMC WITH TWO FBSMs IN WSC AND THE RESULTING CAPACITOR VOLTAGE STATES

Voltage Level (V_x)	Voltages due to different switching combination	Capacitor voltage change	
		$I_x > 0$	$I_x < 0$
V_{dcx}	V_{dcx}	$C_1 \rightarrow C_2 \rightarrow$	$C_1 \rightarrow C_2 \rightarrow$
	$V_{c1} + V_{c2}$	$C_1 \uparrow C_2 \uparrow$	$C_1 \downarrow C_2 \downarrow$
	$V_{dcx} + V_{c1} - V_{c2}$	$C_1 \uparrow C_2 \downarrow$	$C_1 \downarrow C_2 \uparrow$
	$V_{dcx} - V_{c1} + V_{c2}$	$C_1 \downarrow C_2 \uparrow$	$C_1 \uparrow C_2 \downarrow$
$V_{dcx}/2$	$V_{dcx} - V_{c1}$	$C_1 \downarrow C_2 \rightarrow$	$C_1 \uparrow C_2 \rightarrow$
	$V_{dcx} - V_{c2}$	$C_1 \rightarrow C_2 \downarrow$	$C_1 \rightarrow C_2 \uparrow$
	V_{c1}	$C_1 \uparrow C_2 \rightarrow$	$C_1 \downarrow C_2 \rightarrow$
	V_{c2}	$C_1 \rightarrow C_2 \uparrow$	$C_1 \rightarrow C_2 \downarrow$
0	0	$C_1 \rightarrow C_2 \rightarrow$	$C_1 \rightarrow C_2 \rightarrow$
	$V_{dcx} - V_{c1} - V_{c2}$	$C_1 \downarrow C_2 \downarrow$	$C_1 \uparrow C_2 \uparrow$
	$V_{c1} - V_{c2}$	$C_1 \uparrow C_2 \downarrow$	$C_1 \downarrow C_2 \uparrow$
	$-V_{c1} + V_{c2}$	$C_1 \downarrow C_2 \uparrow$	$C_1 \uparrow C_2 \downarrow$
$-V_{dcx}/2$	$-V_{dcx} + V_{c1}$	$C_1 \uparrow C_2 \rightarrow$	$C_1 \downarrow C_2 \rightarrow$
	$-V_{dcx} + V_{c2}$	$C_1 \rightarrow C_2 \uparrow$	$C_1 \rightarrow C_2 \downarrow$
	$-V_{c1}$	$C_1 \downarrow C_2 \rightarrow$	$C_1 \uparrow C_2 \rightarrow$
	$-V_{c2}$	$C_1 \rightarrow C_2 \downarrow$	$C_1 \rightarrow C_2 \uparrow$
$-V_{dcx}$	$-V_{dcx}$	$C_1 \rightarrow C_2 \rightarrow$	$C_1 \rightarrow C_2 \rightarrow$
	$-V_{c1} - V_{c2}$	$C_1 \downarrow C_2 \downarrow$	$C_1 \uparrow C_2 \uparrow$
	$-V_{dcx} - V_{c1} + V_{c2}$	$C_1 \downarrow C_2 \uparrow$	$C_1 \uparrow C_2 \downarrow$
	$-V_{dcx} + V_{c1} - V_{c2}$	$C_1 \uparrow C_2 \downarrow$	$C_1 \downarrow C_2 \uparrow$

HBHMC provides full dc bus utilization compared to the HCMC topology [25], [26], which utilizes only half of the dc-link voltage.

B. Three-phase configuration

To obtain the three-phase output, three HBHMCs (Fig. 1) can be connected either in series (series-HBHMC) or in parallel (parallel-HBHMC). (Figs. 2 (a) and (b)). The three MHBCs of the three-phase converter operate at the fundamental frequency with 120° phase displaced outputs with respect to each other. For series-HBHMC, three separate dc capacitors are required to equally divide the total dc-link voltage (V_{dct}) such that $3V_{dcx} = V_{dct}$ (Fig. 2 (a)). For series-HBHMC, the MHBC outputs are either $+V_{dct}/3$, 0 or $-V_{dct}/3$, and for the parallel-HBHMC the outputs are $+V_{dct}$, 0 or $-V_{dct}$ (Figs. 2(a) and 2(b)). For an N number of series connected FBSMs per phase in WSC, the series-HBHMC capacitor voltage of each SM is regulated to $V_{dct}/3N$, and in the parallel-HBHMC it is regulated to V_{dct}/N . These converters are connected to an ac network through three units of single-phase transformers. These transformers are used

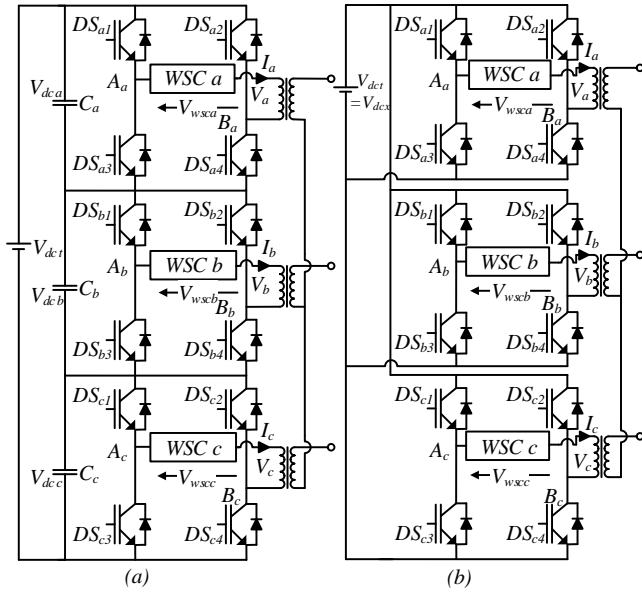


Fig. 2 (a) Illustration of a three-phase series H-bridge hybrid modular converter (series-HBPMC), (b) illustration of a three-phase parallel H-bridge hybrid modular converter (parallel-HBPMC).

to provide isolation between the three-phase outputs of the converter and to match the ac and dc voltage levels [34]. As three separate transformers are used for each phase, it eases the shipment of transformers and also reduces the spare holding requirements. These are important considerations for HVDC applications [34]. As the series-HBPMC uses $1/3$ of V_{dct} for each phase, it is more suitable for the applications like tapping of existing HVDC lines [36], where the dc-link voltage is high and current is low. The parallel-HBPMC uses full V_{dct} for each phase. Hence it is more suitable for applications requiring high current with low dc-link voltage like back to back HVDC system [32] and medium voltage dc transmission system [37].

C. Modes of operation

The normal steady-state HBPMC operation can be categorized into two operating modes depending on the MHBC switching states as explained below.

1) Powering Mode:

In powering mode, the output of MHBC is a square wave and the WSC is responsible to obtain the multilevel output voltage waveform from the output of HBPMC. In this case, the dc-link is connected to load through WSC and it supplies power to both WSC and load. This mode is termed as powering mode because the energy is exchanged between the dc-link and the ac system. In this mode, for the positive half-cycle of output voltage DS_{x1} is on and DS_{x2} is off, and for the negative half-cycle DS_{x1} is off and DS_{x2} is on. Here, x represents phase- a , b , or c . In this mode, the phase- x converter output voltage (V_x) depends on the per-phase dc-link voltage (V_{dct}) and the voltage across WSC (V_{wscx}). For series-HBPMC, $V_{dct} = V_{dct}/3$ and for parallel-HBPMC, $V_{dct} = V_{dct}$. The equivalent circuit schematics for positive and negative half-cycles of the powering mode are shown in Figs. 3 (a) and (b), respectively. From Figs. 1 and 3, V_x and V_{wscx} for N FBSMs in the WSC are expressed as,

$$V_x = (DS_{x1} - DS_{x2})V_{dct} - V_{wscx} \quad (1)$$

$$\text{and } V_{wscx} = \sum_{j=1}^N (S_{j1} - S_{j2}) \times V_{cj} \quad (2)$$

where DS_{x1} and DS_{x2} are the switching states of the MHBC

upper switches of phase- x , S_{j1} and S_{j2} are the switching states of the j^{th} FBSM in the WSC and V_{cj} is the capacitor voltage of j^{th} FBSM in the WSC of phase- x of HBPMC. The MHBC switches DS_{x1} is complementary to DS_{x3} and DS_{x2} is complementary to DS_{x4} . Similarly, S_{j1} is complementary to S_{j3} and S_{j2} is complementary to S_{j4} in j^{th} FBSM of the WSC. For N number of FBSMs in the WSC, if the capacitor voltage of each SM (V_{cj}) is V_{dct}/N then depending on the switching states, the FBSM output voltage is either $+V_{dct}/N$ (positively inserted), $-V_{dct}/N$ (negatively inserted), or zero (bypassed), similar to as that in MHBC.

2) Isolation Mode:

In this mode, the dc voltage source is bypassed and the output current freewheels through MHBC. Henceforth, there is no power exchange between dc-link and ac system. The equivalent circuit diagrams for isolation mode are shown in Figs. 3(c) and (d). These two switching states of MHBC can be alternatively used to have uniform loss distribution among the MHBC switches. The output voltage in this mode is the negative of voltage across the WSC (Figs. 3(c) and (d)) and given by,

$$V_x = -V_{wscx} \quad (3)$$

where V_{wscx} is the voltage across WSC.

It is clear from (1) and (3) that the output voltage can either be the difference of dc-link voltage and the voltage across WSC (powering mode) or just be the voltage across WSC (isolation mode). Thus, for the same number of output voltage levels in powering and isolation modes, if n number of FBSMs of WSC are required to be positively inserted in the powering mode then $(N - n)$ FBSMs of WSC should be negatively inserted in the isolation mode. This implies that, for the same direction of load current and for the same output voltage level, if n number of capacitors of WSC FBSMs are getting charged (discharged) in powering mode, then the $(N - n)$ capacitors of WSC FBSMs get discharged (charged) in isolation mode. This gives an extra degree of freedom for capacitor voltage balancing of WSC SMs, which is achieved without the need of any additional SMs or any zero-sequence component injection. In contrast to this, in HCMC since the isolation mode is not available the SMs capacitor voltage balancing would require extra efforts in terms of using more number of SMs or injecting third harmonic component to the modulation signal [24], [25], [31].

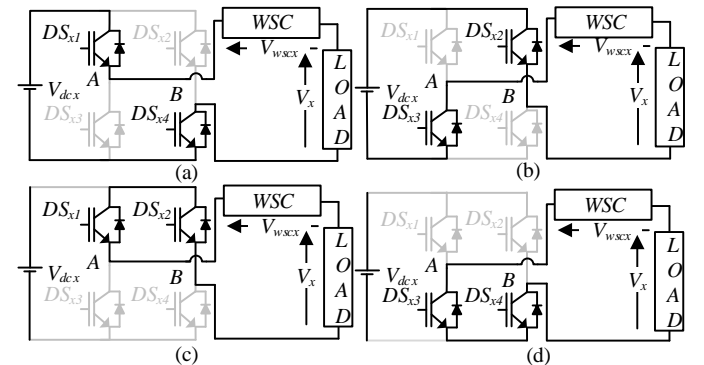


Fig. 3 Equivalent circuit diagrams of HBPMC for different modes of operation (a) positive half cycle of powering mode, (b) negative half cycle of powering mode, (c) and (d) isolation modes.

III. CAPACITOR VOLTAGE BALANCING IN HBPMC

For satisfactory operation of converter it is necessary to have the net active power absorption by WSC to be zero. At the same time the average capacitor voltages of each SMs of WSC should remain equal and constant.

A. Voltage balancing of WSC of HBHMC:

It is assumed that the converter output voltage quality is sufficiently good and the converter switching effects are ignored. The converter phase- x output voltage (V_x) can be expressed as,

$$V_x(t) = V_m \sin(\omega t + \phi_1) \quad (4)$$

where V_m is the phase voltage amplitude, ω is the angular frequency, ϕ_1 is 0, $-2\pi/3$, and $2\pi/3$ for phases a , b , and c , respectively. The output current of phase- x of the converter is assumed to be sinusoidal with the current amplitude of I_m and with an arbitrary phase shift of ϕ_2 and is expressed as

$$I_x(t) = I_m \sin(\omega t + \phi_1 - \phi_2) \quad (5)$$

The modulation index mi of the HBHMC can be expressed as (Fig. 2),

$$mi = \frac{V_m}{V_{dcx}} \quad (6)$$

The instantaneous power flowing through the WSC of phase- x can be expressed as,

$$P_{wscx}(t) = V_{wscx}(t) I_x(t) \quad (7)$$

1) Powering Mode:

From (1) and (4), the WSC voltage of phase- x for powering mode of operation is expressed as

$$V_{wscx}(t) = S_x V_{dcx} - V_m \sin(\omega t + \phi_1) \quad (8)$$

where S_x is 1 when DS_{x1} is on and DS_{x2} is off and it is -1 when DS_{x1} is off and DS_{x2} is on. Substituting the values of I_x and V_{wscx} from (5) and (8) in (7), the instantaneous power of WSC of phase- x is calculated as,

$$P_{wscx}(t) = (S_x V_{dcx} - V_m \sin(\omega t + \phi_1)) I_m \sin(\omega t + \phi_1 - \phi_2) \quad (9)$$

$$\Rightarrow P_{wscx}(t) = V_m I_m \left[\frac{S_x}{mi} \sin(\omega t + \phi_1 - \phi_2) + \frac{1}{2} (\cos(2\omega t + 2\phi_1 - \phi_2) - \cos \phi_2) \right] \quad (10)$$

Integrating (10) over one fundamental cycle yields the following expression of the energy exchange between the WSC and the load (W_{wscx}).

$$W_{wscx} = \int_{-\phi_1/\omega}^{2\pi-\phi_1/\omega} P_{wscx}(t) dt$$

$$\Rightarrow W_{wscx} = \frac{V_m I_m \cos(\phi_2)}{\omega} \left[\frac{4}{mi} - \pi \right] \quad (11)$$

It is clear from (11) that the energy exchanged by the WSC is zero only when $mi = 4/\pi$. For mi other than $4/\pi$ the energy exchanged by WSC is either positive or negative, which will result in increase or decrease of the WSC capacitor voltage, respectively. To make the energy exchanged by WSC equal to zero for $mi < 4/\pi$, the isolation mode of operation is introduced.

2) Isolation Mode:

In this mode, the capacitors of WSC are only supplying power to the ac load and the dc source is bypassed. From (3) and (4), the voltage across phase- x WSC can be expressed as

$$V_{wscx}(t) = -V_m \sin(\omega t + \phi_1) \quad (12)$$

Substituting (5) and (12) in (7), the instantaneous power of phase- x of the converter in isolation mode is calculated as

$$P_{wscx} = (-V_m \sin(\omega t + \phi_1)) I_m \sin(\omega t + \phi_1 - \phi_2) \quad (13)$$

$$P_{wscx}(t) = V_m I_m \left[\frac{1}{2} (\cos(2\omega t + 2\phi_1 - \phi_2) - \cos \phi_2) \right] \quad (14)$$

Hence, the energy exchanged by WSC over one fundamental cycle is calculated as

$$W_{wscx} = \int_{-\phi_1/\omega}^{2\pi-\phi_1/\omega} P_{wscx}(t) dt = -\frac{\pi}{\omega} V_m I_m \cos \phi_2 \quad (15)$$

It is clear from (15) that for the isolation mode the energy exchanged by WSC is always negative regardless of the mi value for powering both the positive and negative half-cycles of output voltage. In the isolation mode the WSC supplies power to load by releasing the energy stored in its FBSMs. By controlling the duration for which the MHBC operates in isolation mode, depending on the current magnitude, the net energy exchanged by WSC in a fundamental cycle can be equated to zero and hence the capacitor voltage balancing can be achieved. Thus, it is evident that the energy exchanged by WSC can be controlled by appropriately selecting powering and isolation modes for $0 \leq mi \leq 4/\pi$. For selecting one of these two operating modes without increasing the switching frequency of MHBC from fundamental, two techniques (HCI and AZCI methods) for capacitor voltage balancing are proposed. The detailed description of these two methods is given below.

a) Half cycle isolation method:

In this method, depending upon the average capacitor voltage of WSC, the HBHMC operates either in powering mode or isolation mode. The mode selection is carried at every zero crossing of output voltage and the selected mode remains active for the next half of the fundamental cycle. Thus the MHBC operates at fundamental frequency, which keeps the switching losses of MHBC to minimal. For the HCI mode selection, as shown in Fig. 4(a), the average capacitor voltage of the WSC SMs (V_{avg}) is obtained. At every zero crossing of the reference output voltage (V_{xref}), this average capacitor voltage is compared with the reference capacitor voltage (V_{refavg}), which is set to the V_{dcx}/N . If V_{avg} is less than V_{refavg} then the powering mode is selected by turning on the MHBC switches D_{x1} and D_{x4} , D_{x2} and D_{x3} for positive and negative cycles of output voltage, respectively. On the other hand, if V_{avg} is greater than V_{refavg} then isolation mode is selected by turning on the MHBC switches (either D_{x1} and D_{x2} or D_{x3} and D_{x4}). The mode selection is performed in the manner as shown in Fig. 4(a). The voltage waveform at the different stages of converter are shown in Fig. 4(b). As the converter operates in powering mode or isolation mode, at least for half of the fundamental cycle the capacitors of WSC SMs continue to charge or discharge for half cycle although the average WSC SMs voltage is changed from its initial state. Next change of mode is selected only at next zero crossing of output voltage. This increases the fluctuations of capacitor voltages and hence capacitor value of WSC SMs [40]-[43]. Moreover, in this method during the isolation mode, only WSC is generating output and with N FBSMs the maximum output voltage obtained from the WSC is V_{dcx} . This restricts HBHMC to operate in the overmodulation region where the peak of per phase output voltage should be greater than V_{dcx} . Hence in this method additional SMs are required for the HBHMC to operate in the overmodulation region.

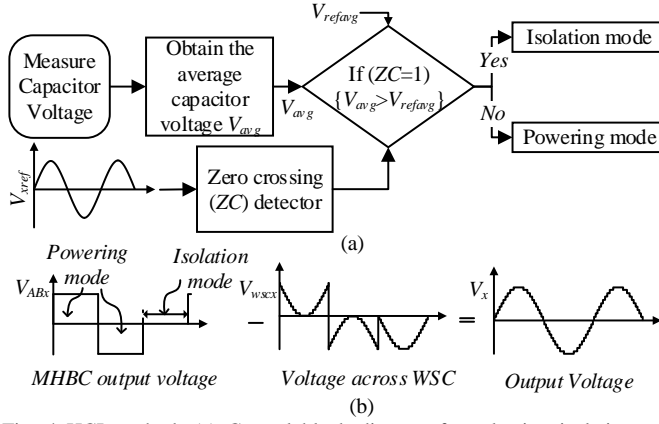


Fig. 4 HCI method; (a) Control block diagram for selecting isolation and powering modes, and (b) Voltage waveforms at different stages of HBHMC.

b) Across zero crossing isolation method:

In this method, instead of keeping the isolation mode active for complete half of the fundamental cycle, which increases the capacitor voltage fluctuation as discussed above, it is activated only across the zero crossing of output voltage. A control block diagram illustrating this method is shown in Fig. 5(a). In this method, to decide the time duration for which the isolation mode is active the average capacitor voltage of WSC (V_{avg}) is compared with reference voltage (V_{refavg}). This error is passed through a PI controller as shown in Fig. 5(a) and output of PI controller (e) is compared with output voltage reference (V_{xref}) to obtain the isolation and powering mode signals. The output voltage waveforms of converter at different stages of converter are shown in Fig. 5(b). The converter output voltage (V_x) with reference to Fig. 1 is given as

$$V_x = V_{ABx} - V_{WSCx} \quad (16)$$

where V_{ABx} is the output voltage of MHBC. V_{ABx} is $+V_{dcx}$ for positive half cycle and $-V_{dcx}$ for negative half cycle. If the voltage across WSC is positive (positively inserted) in positive half cycle and negative (negatively inserted) in the negative half cycle then the output voltage will always be less than V_{dcx} , i.e. the dc-link voltage for each phase. However, if the voltage across WSC is negative in positive half cycle and positive in negative half cycle then the output voltage can be greater than V_{dcx} . This is because the WSC voltage gets added to the dc voltage to obtain the output voltage, as described above by (16). As the maximum voltage across the WSC is kept at V_{dcx} , the converter operation can ideally be extended up to the modulation index of 2. However, to keep the net energy exchanged by WSC capacitors to be zero and hence maintain the capacitors voltage constant, as explained earlier in Sec. III-A, the maximum modulation index is restricted to $4/\pi$. This indicates that, by using the AZCI method the HBHMC can be operated in the overmodulation region without the need of additional SMs in the WSC.

In both HCI and AZCI methods, during the isolation period the load current is supplied by WSC and the dc-link capacitor is bypassed. For three-phase HBHMC, the isolation mode of operation for each phase depends on the WSC capacitor voltage of that particular phase and becomes active only if the WSC capacitor voltage is greater than the reference value. Thus the isolation periods in all the three phases may or may not be active simultaneously. When the isolation period of a particular phase is active the dc-link capacitor of that phase is bypassed and only WSC supplies power to load. In case of half cycle

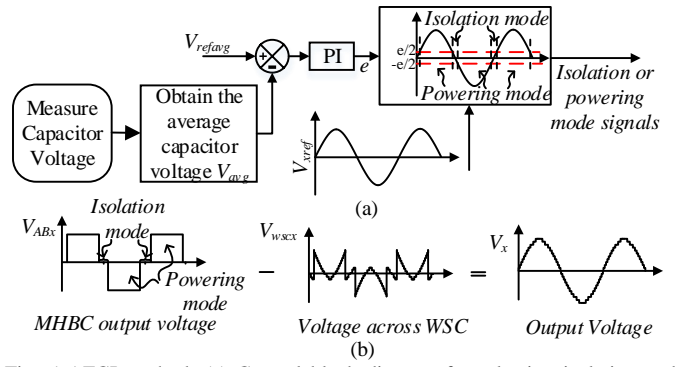


Fig. 5 AZCI method; (a) Control block diagram for selecting isolation and powering modes, and (b) Voltage waveforms at different stages of HBHMC.

isolation (HCI) method, the isolation period is active for half cycle. During this period the isolation modes of other two phases may or may not be active. For the series-HBHMC, during isolation interval of one phase, if the other two phases are in powering mode (isolation modes are not active), the current flowing through dc-link capacitor of that phase (the phase for which isolation mode is active) is the sum of currents of other two phases. Thus this capacitor is handling two phase power. So the capacitor size requirement is more as compared to that in the converter operating without isolation mode [43]. However, for the across zero crossing isolation (AZCI) method, the isolation period is small and occurs only across the voltage zero crossing. For a three-phase system, the isolation period comes after every 60 degrees as shown in the Fig. 6. Fig. 6 shows the three-phase reference signals and corresponding isolation signals for AZCI method. In Fig. 6, when the isolation signal of a particular converter phase is high then that phase operates in the isolation mode. On the other hand, the corresponding converter phase operates in powering mode when its isolation signal is zero. For small isolation period in the AZCI method the capacitor size requirement is less as compared to the HCI method but more than the capacitance requirement for system without isolation.

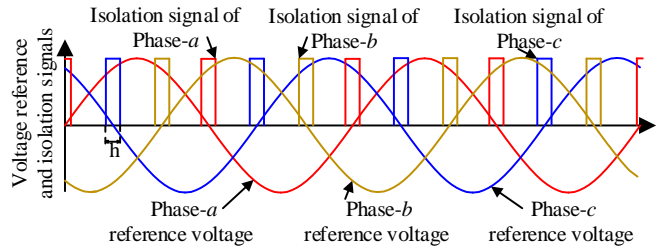


Fig. 6 Three-phase output voltage references and corresponding isolation signals for AZCI method.

B. Individual FBSM capacitor voltage balancing in WSC

As explained in the previous subsection, it is possible to keep the average capacitor voltage of WSC constant by properly selecting isolation and powering modes of operation for HBHMC. However, it does not guarantee equal capacitor voltages for all FBSMs. At every change in the converter output voltage level when a SM is either required to be inserted or bypassed, if any arbitrary SM is chosen then some of capacitors can get overcharged and some discharged as the energy will not be evenly distributed among all of them. To maintain each capacitors voltage equal, a sorting and insertion technique for HBHMC is proposed with the flow chart shown in Fig. 7. In this technique, all SMs capacitor voltages are first measured and they are sorted in ascending or descending order as shown in Fig. 7. Then the converter mode selection is performed in the

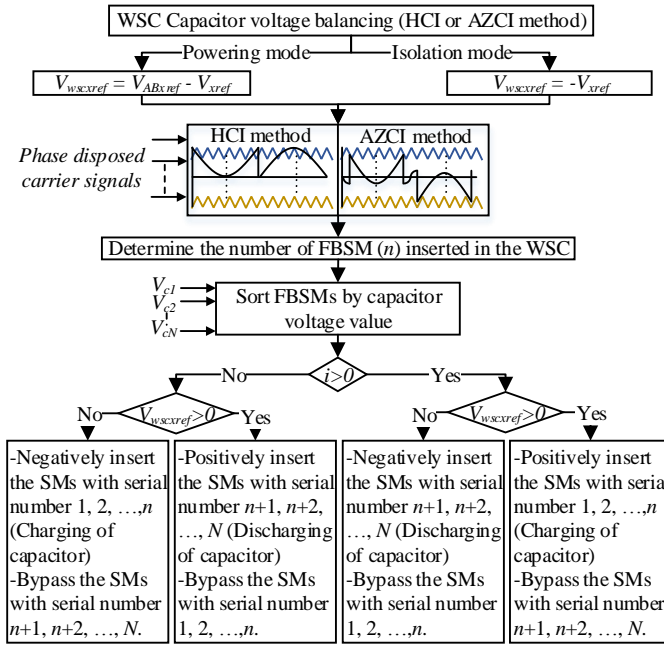


Fig. 7. Flow chart of sorting and obtaining gate signals of FBSM of WSC.

manner as explained in the previous subsection. Depending on the converter mode of operation the WSC voltage reference signal ($V_{wscxref}$) is obtained. For powering mode of operation of the converter, $V_{wscxref}$ is obtained by subtracting the converter output voltage reference signal (V_{xref}) from the MHBC output voltage reference (V_{ABxref}). For isolation mode of operation $V_{wscxref}$ is the negative of V_{xref} (Figs. 3 – 5). After obtaining the reference signal $V_{wscxref}$, it is compared with the phase-disposed triangular carrier signals (since the phase disposition strategy provides the lowest line-to-line total harmonic distortion [38], [39]), to calculate the required number of FBSMs to be inserted (n) in the WSC. If $V_{wscxref}$ is positive then n number of FBSMs are inserted positively to obtain the desired positive voltage across the WSC. Similarly, n FBSMs are negatively inserted if $V_{wscxref}$ is negative to obtain the desired negative voltage across the WSC. Assuming all the capacitor voltages are sorted from the low to high value and the corresponding FBSMs are numbered in ascending order then, depending on the current direction, the insertion or bypassing of the SMs are performed in the manner as illustrated in Fig. 7. Thus, this technique ensures equal charge distribution over all the SM capacitors.

IV. HBHMC VALIDATION AND APPLICABILITY TO HVDC SYSTEM

A. Standalone mode

To validate the effectiveness of the proposed converter and its associated control schemes, a standalone model of series-HBHMC with two FBSMs ($N = 2$) per phase (Fig. 1) is simulated using PSCAD. The simulation parameters are listed in Table III. The capacitance values of FBSMs and dc-link are selected such that the maximum voltage deviation is 10% of their respective reference voltage values [40]–[43], [45]. These capacitor values of SMs result in the capacitance energy storage of 25 kJ/MVA and 5.2 kJ/MVA for HCI and AZCI methods, respectively. Moreover, this also results in the dc-link capacitance energy storages of 15.75 kJ/MVA and 12 kJ/MVA for HCI and AZCI methods, respectively. Thus, the capacitance energy storage is higher for HCI method as compared to AZCI method as discussed earlier in Sec. III A. It is also clear from these values that a significant reduction in the net capacitance

TABLE III
PARAMETERS OF THE SIMULATED SYSTEM

Sr. No.	Parameter	Value
1.	dc-link voltage (V_{dc})	450 V
2.	Submodule voltage	75 V
3.	No of submodules/Phase	2
4.	Submodule Capacitance	
	For HCI method	177 μ F
	For AZCI method	36 μ F
5.	dc-link capacitance/phase	
	For HCI method	56 μ F
	For ACZI method	40 μ F

energy storage requirement is achieved in the proposed converter controlled using the AZCI method as compared to that in the MMC, which requires the capacitance energy storages of 39 kJ/MVA [43].

The series-HBHMC is operated with $mi = 0.95$ and with a passive R - L load of 0.9 power factor at 50 Hz. The converter modulation is performed using PDPWM technique [38], [39], with a carrier frequency of 2 kHz. Figs. 8 and 9 show the simulation results of series-HBHMC system controlled using the HCI (Fig. 4), and the AZCI methods (Fig. 5), respectively. It can be observed from these waveforms that the proposed control schemes are able to effectively balance the capacitor voltages and hence distinct five-level phase-voltage waveforms are generated at the converter output. The series-HBHMC output voltage and output current waveforms using the two abovementioned proposed control schemes are plotted in Figs. 8(a) and 9(a) respectively. Figs. 8(b) and 9(b) show the modulation signals used to obtain gate pulses for the FBSMs in HCI and AZCI methods, respectively (Sec. III). It can be seen from Figs. 8(b) and 9(b) that, as discussed in the previous section (Figs. 4 and 5), the isolation period is active over half cycle for HCI method and across zero crossing for AZCI method, respectively. The switching signals of the upper two switches (DS_{x1} and DS_{x2}) of MHBC for HCI and AZCI methods are shown in Figs. 8(c) and 9(c), respectively. The switch DS_{x3} is complimentary to DS_{x1} and DS_{x4} is complimentary to DS_{x2} . It can be seen from Figs. 8(c) and 9(c) that the MHBC switches are switched at the fundamental frequency (50Hz in this case), which helps in keeping the switching losses of the converter to minimal. Figs. 8(d) and 9(d) show the capacitor voltages of WSC with and without the proposed voltage control scheme for HCI and AZCI methods, respectively. With reference to Figs. 8(d) and 9(d), in the initial period of the simulation the HBHMC is operated without using the proposed capacitor voltage control methods, and at t_1 the proposed voltage controllers are activated. It can be observed that the WSC capacitor voltages tend to become unbalanced when the control is inactive and they settle at the reference value (half of the per phase dc-link voltage, i.e., 75 V) after the control is activated, which validates the effectiveness of the proposed control techniques.

To validate the overmodulation capability of HBHMC, the series-HBHMC is simulated for $mi = 1.2$ and the corresponding three-phase converter output voltage and current waveforms are shown in Figs. 10(a) and (b), respectively. Here, the AZCI method is used for controlling the WSC capacitors voltage. The modulation signals for phase- a using the AZCI method are shown in Fig. 10(c). It can be observed from Fig. 10(c) that around the peak of output voltage reference, the reference signal of WSC is negative in the positive half cycle and positive in the negative half cycle of output voltage reference. This is done to obtain the converter output voltage greater than V_{dc} , as explained earlier in Sec. III-A (Fig. 5). It can be seen From Fig.

10 (a) that the number of output voltage levels have increased from five (for $mi \leq 1$) to seven because of the overmodulation mode of operation. Moreover, the converter output voltage magnitude has also increased as can be seen by comparing Fig. 10 (a) with Figs. 8 (a) and 9 (a). It is also to be noted that, like in the undermodulation region ($mi \leq 1$), in the overmodulation region too ($mi > 1$), the WSC is modulated at the frequency of

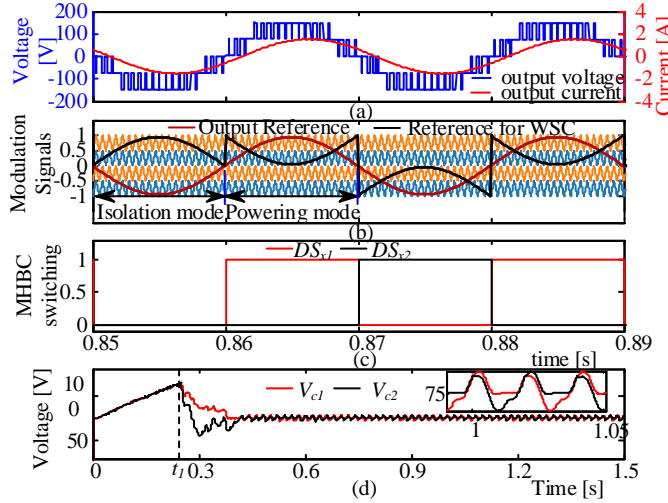


Fig. 8 Waveforms of HBHMC using HCI method (a) Output voltage and current waveforms, and (b) Modulation signals for HCI method, (c) switching signals of MHBC, and (d) individual capacitor voltages of WSC.

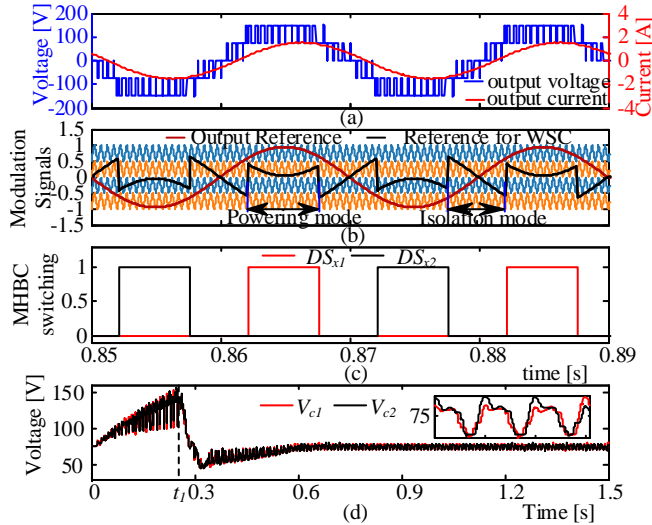


Fig. 9. Waveforms of HBHMC using AZCI method (a) output voltage and output current waveform, (b) Modulation signals for ACZI method, (c) switching signals of MHBC, and (d) Individual capacitor voltages of wave shaping circuit.

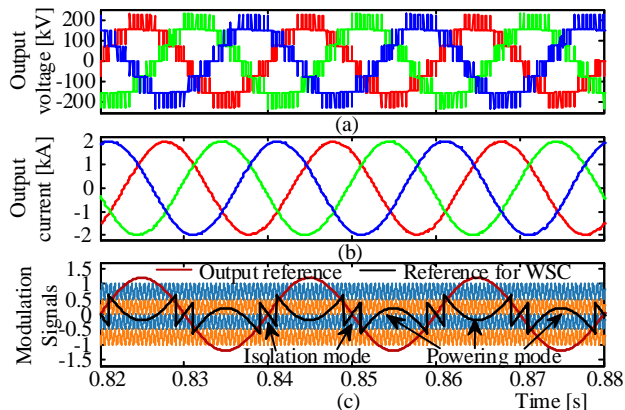


Fig. 10. Series-HBHMC operating at $mi = 1.2$ (a) three-phase output voltage waveforms and, (b) three-phase output current waveforms (c) modulation signals for ACZI method.

the carrier signals, as can be seen from Figs. 8-10. Hence the converter output voltage waveform quality does not deteriorate even in the overmodulation region.

The simulation results presented in Figs. 8-10 validate the efficacy of the proposed control techniques and the operation of series-HBHMC. The parallel-HBHMC can also be simulated using the proposed control techniques to obtain similar results.

B. Applicability of series-HBHMC for HVDC system

To test the proposed HBHMC for HVDC application a test model is built in PSCAD/EMTDC using series-HBHMC with the schematic shown in Fig. 11(a). The simulation parameters are listed in Table IV. The dc-link voltage (V_{dc} , Fig. 2 (a)) for each phase of converter is 50 kV ($V_{dc}/3$). The converter uses 10 FBSMs per phase with the voltage rating of 5 kV ($V_{dc}/3N$). The control of HBHMC based HVDC system can be sectionalized in three different layers, i.e., inner, intermediate and outer control layers, as shown in Fig. 11 (b) [26], [30]. The outer control layer includes the dc-link voltage (or active power) controller and the reactive power (or ac voltage) controller. These controllers provide the reference values to the current controllers in the intermediate control layer. As it is known that in a VSC-HVDC system one of the converter stations is controlled to follow an active power flow reference while the other station is controlled to regulate the dc-link voltage around its reference value. Therefore, depending on the converter station under consideration, the current reference i_d^* is generated either by an active power controller or the dc-link voltage controller. Another current reference i_q^* is generated either by the ac voltage controller or by the reactive power controller. In the intermediate control layer, the reference currents output from the external control layer are compared with their actual values, i_d and i_q , respectively and the errors are processed through PI controllers. The outputs of this control layer are V_d and V_q , which when converted back to the abc frame provides the modulation signals for the converter. The inner control layer is the capacitor voltage control technique proposed earlier in Sec. III. Here, the AZCI method is used to control WSC capacitor voltage because of its advantages over HCI method, such as, smaller value of submodules capacitance and overmodulation capability. This control layer balances the overall capacitor voltage and individual SM capacitor voltages and generates the gate pulses for WSC SMs and MHBC. The control scheme shown in Fig. 11 (b) can also be used for parallel-HBHMC based HVDC system.

1) Series-HBHMC HVDC System Operation:

The series-HBHMC HVDC system of Fig. 11(a), with the different control layers shown in Fig. 11(b), is simulated for a balanced three-phase system to test its performance under active and reactive power control and power reversal modes of operation in this subsection. At converter station 1 (CS1), the active and reactive power outputs of the converter are being controlled, while at converter station 2 (CS2), the dc-link voltage and the reactive power control actions are being implemented. Fig. 12 shows the simulation results obtained when, at $t = 0.5$ s, the active power flow direction of CS1 is reversed, i.e. P_s^* is changed from -150 MW to $+150$ MW. The change rate of P_s^* is 1.2 MW/ms. The resulting active power waveforms at the output terminals of CS1 and CS2 are shown in Fig. 12(a). The corresponding three-phase ac output currents are shown in Fig. 12(b). Figs. 12(c) and 12(d) show the dc-link capacitor voltages of CS1 and CS2, respectively. These

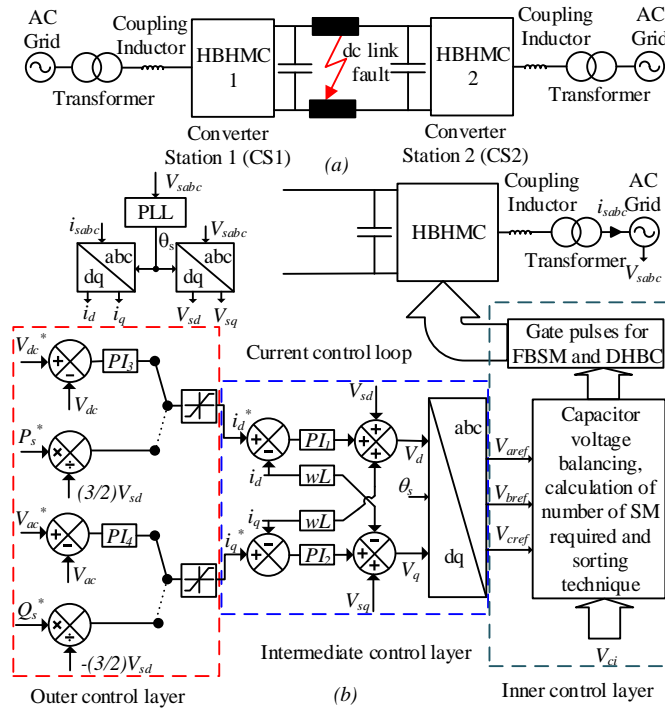


Fig. 11. (a) Schematic of HVDC system (b) Control block diagram of converter for HVDC system

TABLE IV

PARAMETERS OF THE STUDY HBHMC-HVDC SYSTEM

Sr. No.	Parameter	Value
1.	dc-link voltage (V_{dcl})	150 kV
2.	Submodule voltage	5 kV
3.	No of submodules/Phase	10
4.	dc-link capacitance	150 μ F
5.	Submodule Capacitance	0.5 mF
6.	Grid voltage for HVDC	220 kV
7.	Single phase transformer voltage rating	127kV/35kV

capacitor voltages are equal to one third of the total dc-link voltage. Moreover, the phase-*a* WSC capacitor voltage waveforms of CS1 and CS2 are shown in Figs. 12(e) and 12(f), respectively. It can be observed from Fig. 12 that the power reversal is achieved with minimum transients in ac output currents, dc-link capacitor voltages, and WSC capacitor voltages of the converter. At $t = 1.0$ s, the reactive power reference of CS1 (Q_s^*) is changed from -100 MVar to $+100$ MVar, with 1.2 MVar/ms slope. The waveforms of active and reactive powers at the output terminals of CS1 are shown in Fig. 13(a) and the corresponding dc-link capacitor voltage waveforms and phase-*a* WSC capacitor voltage waveforms are shown in Figs. 13(b) and 13(c), respectively. Similarly, at $t = 1.5$ s, the reactive power reference of CS2 is changed from $+100$ MVar to -100 MVar and resulting waveforms of active and reactive powers at the converter output terminals, dc-link capacitor voltage waveforms, and phase-*a* WSC capacitor voltages of CS2 are shown in Figs. 14(a), 14(b), and 14(c), respectively. The results shown in Figs. 12, 13, and 14 verify the effectiveness of the proposed control schemes and satisfactory performance of the HBHMC based HVDC system in response to the active and reactive power reversal commands. It is also observed that the FBSMs capacitor voltages are well regulated and balanced at their reference values in all cases.

2) Control of series-HBHMC HVDC System under dc fault condition:

One of the important characteristics of HBHMC is its ability to block dc fault current. As the HBHMC uses FBSMs, it is possible to apply an opposite polarity voltage in the event of a dc side fault, thereby limiting/blocking the fault current magnitude. The intended ability of the HBHMC to block the dc fault current is tested for the worst case scenario by creating a pole-to-pole dc side fault (Fig. 11). As soon as the fault is detected the IGBTs are turned off. The resulting equivalent circuits for positive and negative half-cycles of the grid voltage are shown in Figs. 15 (a) and (b), respectively. In both these cases, for the chosen system parameters (Table IV), since the net WSC capacitor voltage is greater than the grid voltage, the antiparallel diodes connected across the IGBTs in the WSC get reverse biased (Fig. 15) and hence the flow of current is ceased. Fig. 16 shows the results when the system is subjected to the pole-to-pole dc fault (Fig. 11(a)). Before the fault occurrence the system of Fig. 11(a) is in steady state condition and is controlled to operate with $P_s^* = 150$ MW and $Q_s^* = 100$ MVar at CS1 (Fig. 11 (b)). It can be seen from Fig. 16(a) that the corresponding CS1 power references are being tracked before 0.5 s in the simulation run. At $t = 0.5$ s, a dc side pole-to-pole short circuit fault is created, which lasts for 200 ms. Following the fault occurrence, it can be observed from Fig. 16 (a) that the active and reactive powers exchange between the converter and ac grid reduces to zero. This is because of turning off of all of the converter switches, which consequently activates the converter inherent dc fault blocking capability as can be observed from the resulting equivalent circuit shown in Fig. 15. It can further be seen from Fig. 16 (b), where the converter three-phase current waveforms are plotted, that the converter phase currents are reduced to a very small value during the fault condition. This confirms the effectiveness of the proposed converter in blocking the dc fault current. Fig. 16 (c) shows the converter dc side voltage, which expectedly collapses to zero during the fault period. Fig. 16 (d) shows the capacitor voltages of FBSMs in phase-*a*, which have negligible ripple and remain constant because the current is blocked. After the fault is cleared at $t = 0.7$ s, the gating signals of switches of both the converter stations are de-blocked and the reference power settings (P_s^* , Q_s^* , Fig. 11 (b)) are ramped up gradually from 0 to the pre-fault values. This allows the converter active and reactive powers exchange with the grid to be ramped up gradually from zero to their pre-fault values as can be seen from Fig. 16 (a). It can be observed from Fig. 16 (b) that the converter experiences inrush currents for a short period of time when the converter is de-blocked. These relatively higher value of current flows because of the charging of dc-link capacitors after the fault is cleared. It can also be observed from Fig. 16 that the pre-fault operating conditions are restored using the control action (Fig. 11 (b)) after the fault is cleared.

It can be concluded from above that even though the test system is subjected to the most severe type of dc fault, the ac grid contribution to the dc side fault current is blocked by the converter control action and the risk of converter failure because of high current stresses is reduced.

3) Control of series-HBHMC HVDC System under grid voltage unbalance condition:

In the previous sections, the simulations of HBHMC were presented by assuming balanced three-phase grid conditions. With reference to the series-HBHMC circuit (Fig. 2 (a)), the three dc capacitor voltages (V_{dca} , V_{dcb} , V_{dcc}) of the three

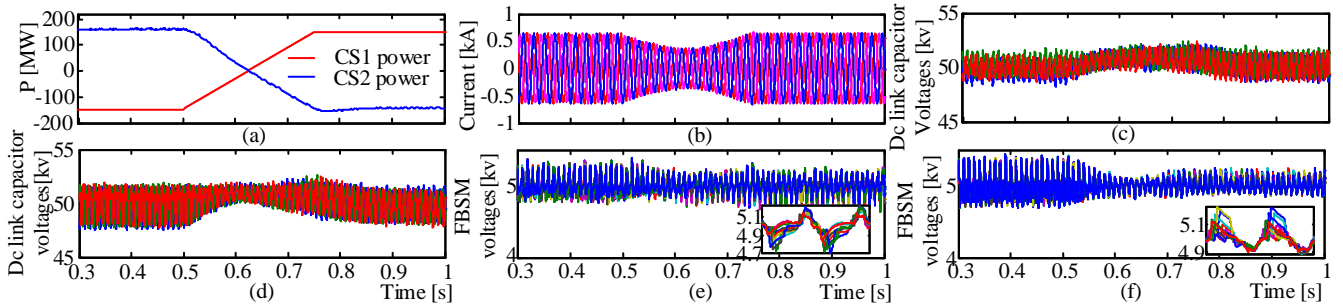


Fig. 12. Responses of converter for HVDC system when active power flow is reversed from -150MW to 150MW at CS1 (a) active power at CS1 and CS2, (b) three-phase ac grid currents at CS1, (c) CS1 dc-link voltages, (d) CS2 dc-link voltages, (e) capacitor voltages of FBSMs of WSC of phase-a at CS1, and (f) capacitor voltages of FBSMs of WSC of phase-a at CS2.

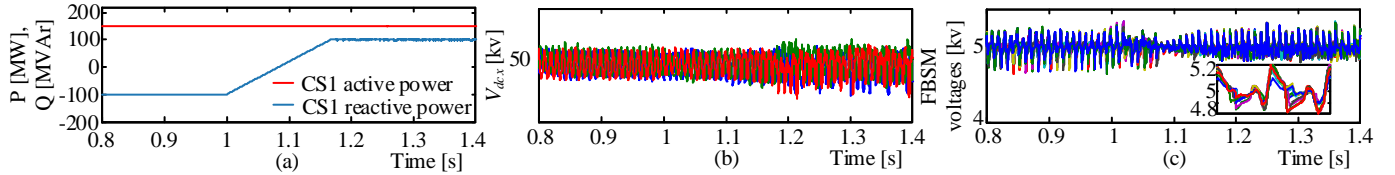


Fig. 13. (a) Active and reactive power waveforms of CS1 when reactive power is changed from -100MW to 100MW, (b) dc-link capacitor voltages, and (c) capacitor voltages of WSC.

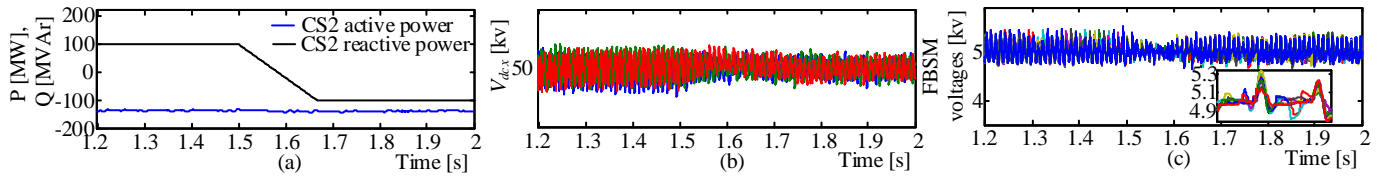


Fig. 14. (a) Active and reactive power waveforms of CS2 when reactive power is changed from 100MW to -100MW, (b) dc-link capacitor voltages, and (c) capacitor voltages of WSC.

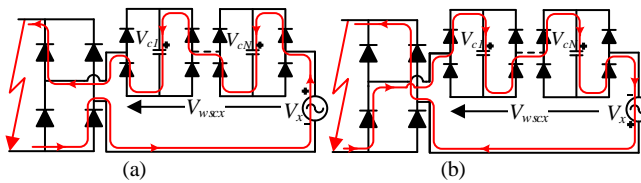


Fig. 15. HBHMC during dc fault, (a) Single-phase equivalent diagram of HBHMC for positive grid voltage, (b) Single-phase equivalent diagram of HBHMC for negative grid voltage.

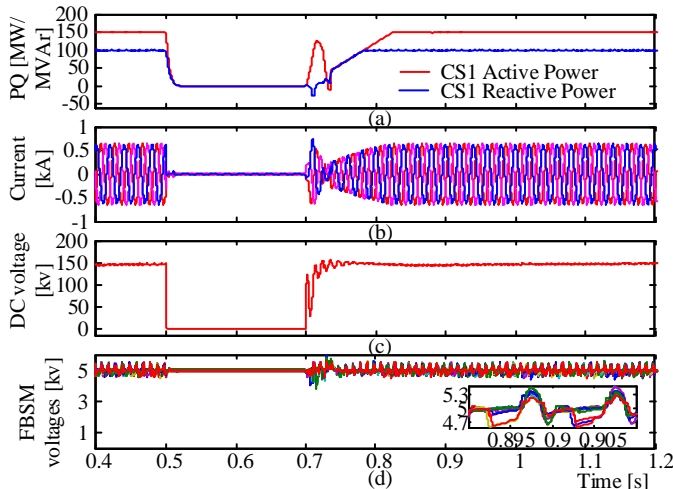


Fig. 16. Responses of CS1 when dc fault occurs during 0.5 to 0.7 sec (a) active and reactive power at the time of dc side fault, (b) ac current during dc side fault, (c) dc-link voltage during dc fault, and (d) FBSM capacitor voltages of phase-a.

individual phases, would depend on the respective magnitudes of power transferred to the grid. For a balanced three-phase system the power transferred by each phase is same and equal to one third of the total power transferred. Hence, the dc capacitors would be having the same average steady state voltage values. However, in certain conditions, the grid voltage can be unbalanced. In such cases the control scheme presented

in [46]-[47] can be applied for the HBHMC. In the simulation study presented here, to control the WSC capacitor voltages the AZCI method, as explained earlier in Section III, is used. In order to investigate the transient response of the dc-link capacitor voltages of the series-HBHMC under unbalance grid voltage, the phase-a grid voltage is reduced to one third of its nominal value at $t = 2.0$ s and it lasts for 3 s. Figs. 17 and 18 show the transient behavior of the system during the grid voltage unbalance. Fig. 17 (a) shows the three-phase grid voltages following the event of occurrence of unbalance at $t = 2.0$ s. When the HBHMC is subjected to the grid voltage unbalance and no post-unbalance control is activated (i.e., from $t = 2.0$ to 3.0 s), the ac-side currents (Fig. 17(b)) and dc capacitor voltages (Fig. 18(b)) of the series-HBHMC become unbalanced before $t = 3.0$ s. This is due to the presence of non-zero negative sequence current components. Thus, in the proposed grid-connected series-HBHMC, there are two control objectives to be exercised in order to deal with this issue. The first objective is to make the converter output current balanced and the second is to equalize the dc capacitor voltages of each phase. The converter current can be balanced by introducing a negative sequence current controller, as described in [47] for the modular multilevel converter. A similar control scheme has been implemented in the presented work for the same objective and it can be seen from Fig. 17(b) that as soon as the said controller is applied at $t = 3.0$ s in the simulation run, the converter currents attain balanced condition. When the post-unbalance control is active, the negative sequence current components are reduced to zero and the ac-side currents of Fig. 17(b) are balanced. It can be seen from Figs. 17(b) and 18(b) that although the ac side currents remain balanced by the virtue of a negative sequence current controller, the dc-link capacitor voltages are still unbalanced (i.e., from $t = 3.0$ to 4.0 s). Similar issue of unbalanced dc capacitor voltages for parallel hybrid

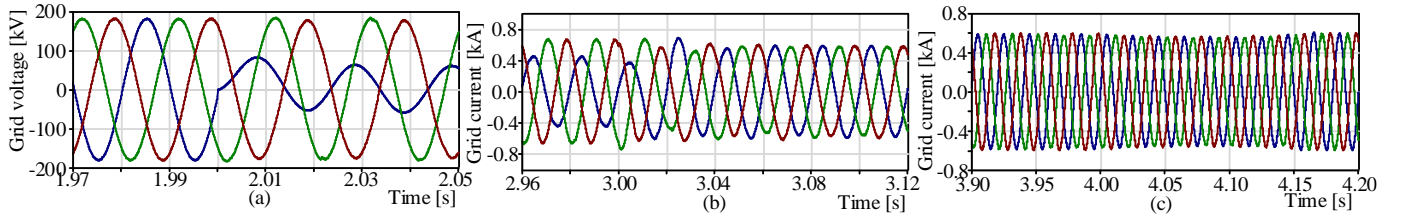


Fig. 17. (a) Unbalance in grid voltage at $t = 2.0$ s, (b) grid currents when positive and negative current control is activated at $t = 3.0$ s, and (c) grid currents when dc capacitor voltage control is activated at $t = 4.0$ s.

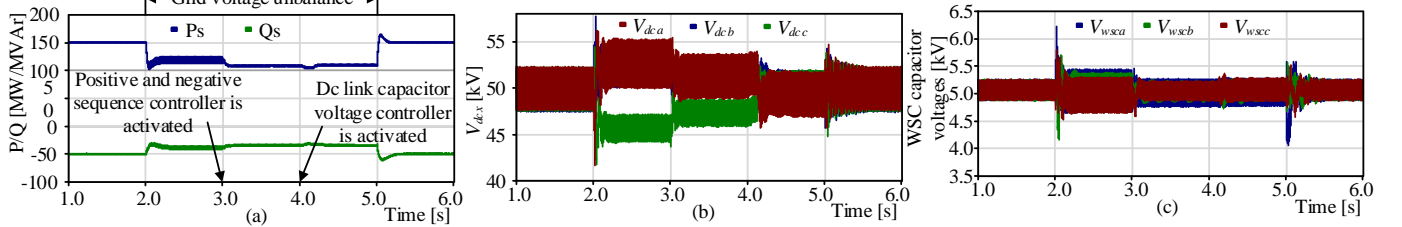


Fig. 18. Response of the series-HBHC to ac side unbalance voltage: (a) active and reactive power, (b) dc-link capacitor voltages, and (c) average values of WSC capacitor voltages.

converter was discussed in [46] and a third harmonic injection based control scheme was used for balancing the dc capacitor voltages under similar unbalanced grid conditions. Therefore, in order to equalize these dc capacitor voltages of the proposed series-HBHC a control technique similar to the one discussed in [46] is used. It can be observed from Fig. 18(b) that as soon as the said controller is activated at $t = 4.0$ s in the simulation run, the capacitor voltages are equalized. Fig. 17(c) also demonstrates that the converter current remain balanced after the activation of both the additional controllers. Hence both the control objectives have been fulfilled. Fig. 18(c) shows the average values of three-phase WSC capacitor voltages, which validates the effectiveness of the proposed voltage control technique (AZCI method) even under unbalance grid conditions. Fig. 18(a) shows the active and reactive power transferred by the HBHC to grid. The active and reactive powers are reduced because the current references are limited to avoid overcurrent in the converter.

V. EXPERIMENTAL VALIDATION

This section presents the experimental results for the three-phase grid-connected HBHC prototype built in the laboratory with two FBSMs per phase in the WSC. Fig. 19 shows the HBHC converter lab prototype. The main experimental parameters are listed in Table V. The converter is modulated using PDPWM technique with the carrier frequency of 2.0 kHz and the grid frequency is 50 Hz. The control and modulation technique are implemented using TMS320F28335 DSP microcontroller. The block diagram of the implemented system hardware configuration is shown in Fig. 20. The intermediate and inner control layers shown earlier in Fig. 11 (b) are also used for the experimental studies. The current references (i_d^* and i_q^*) are set by the system operator. The AZCI method (Fig. 5) is used to control the WSC capacitor voltage and the current control loop (intermediate control layer, Fig. 11 (b)) is used to regulate the active and reactive current components. Figs. 21 and 22 show the steady state experimental results of balanced three-phase grid-connected series-HBHC and parallel-HBHC, respectively, when the converters are controlled to operate in the overmodulation mode. The converters are controlled to supply power to the three-phase grid at a lagging power factor. It can be observed from Figs. 21(a) and 22(a) that the total capacitor voltage of the WSC (in phase-a) is maintained at 150 V and the individual capacitor

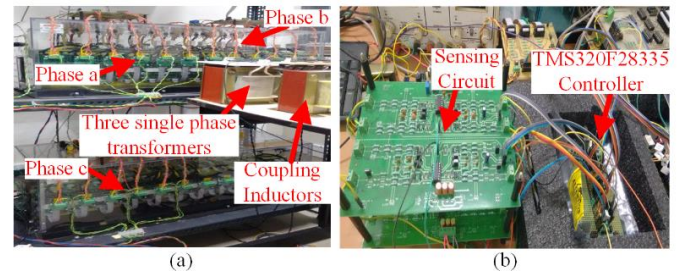


Fig. 19. Picture of experimental prototype (a) a three-phase HBHC with two FBSMs per phase in the WSC, and (b) sensing circuits and DSP controller.

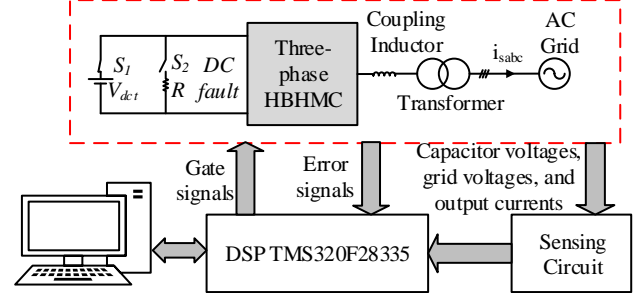


Fig. 20. Architecture of control system implementation for the HBHC

Parameters	Values
Power rating	2KVA
dc-link voltage	450V
Series-HBHC	150V
Parallel-HBHC	150V
No. of FBSMs per phase	2
FBSM voltage	75V
FBSM capacitance	2.0 mF
Single-phase transformer turns ratio	1:1.3

voltages are maintained at 75 V each for both series and parallel configurations using the proposed control technique.

Figs. 21(a) and 22(a) also show the steady state three-phase converter output voltage and current waveforms for series-HBHC and parallel-HBHC, respectively. The converter produces seven level voltage waveforms, which reconfirms its effectiveness in operating in the overmodulation mode, as also observed in the simulation studies discussed earlier in Sec. IV (Fig. 10). It can also be seen from Figs. 21(a) and 22(a) that the FBSMs capacitor voltages are nearly equal and maintained constant at 75 V, which validates the proposed voltage control

and sorting techniques presented earlier in Sec. III. The waveforms of MHBC output voltage, voltage across WSC, converter output current, and the grid voltage of phase-*a* for series and parallel HBHMC using the AZCI method are shown in Figs. 21(b) and 22(b), respectively. It can be observed from the waveform of voltage across WSC that the isolation mode is active only across the zero crossing of output voltage, as expected for the AZCI method.

Fig. 23 shows the dynamic performance of the series-HBHMC for output current change. Fig. 23(a) shows the results of output current, grid voltage, capacitor voltages of WSC for step change in current magnitude at unity power factor. Similarly, Figs. 23(b), (c), and (d) show the results for step current change from unity to lagging power factor, unity to leading power factor, and lagging to leading power factor, respectively. It is clear from these results that the converter

operates satisfactorily and without any significant transient for a wide range of operating conditions. The references are tracked pretty smoothly even when a change in reference magnitude/phase is applied.

Fig. 24 shows the waveforms of three-phase converter output voltages, output current, grid voltage of phase-*a*, and WSC capacitor voltages (phase-*a*) when both the magnitude and phase of the reference current are changed at the same time. This change in current references resulted in a reduced value of m_i , which henceforth changed the converter operation from overmodulation to undermodulation mode. It can be seen from Fig. 24 that the number of output voltage levels have decreased from seven (for $m_i > 1$) to five because of the undermodulation (for $m_i \leq 1$) mode of operation. Similarly, Fig. 25 shows the waveforms of converter output voltages, output current, grid voltage and dc-link capacitor voltage for load current change.

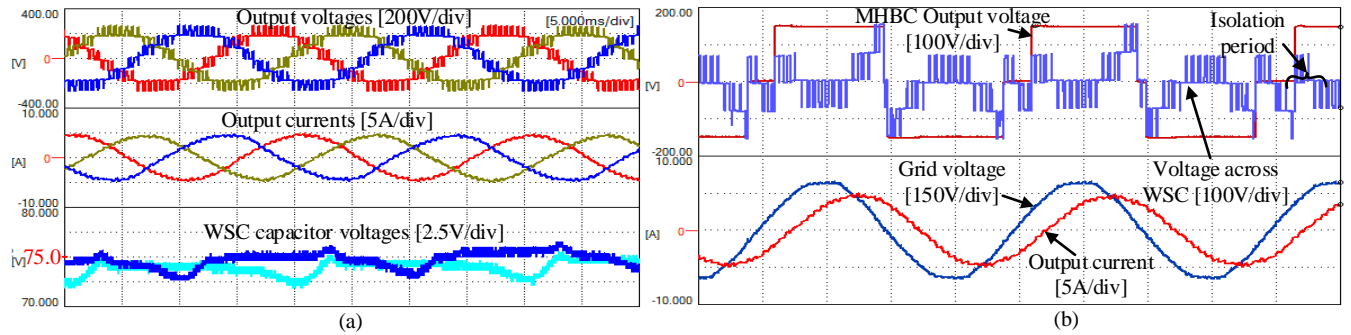


Fig. 21. Experimental steady state output waveforms of series-HBHMC with AZCI method, (a) three-phase output voltages, output currents, and two FBSM capacitor voltages of phase-*a*, (b) Output voltage of MHBC, corresponding voltage across WSC, phase-*a* current, and grid voltage.

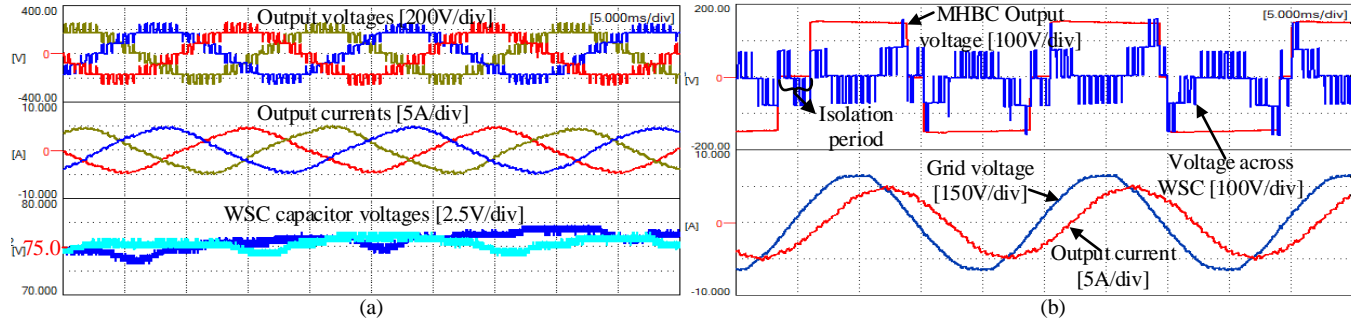


Fig. 22. Experimental steady state output waveforms of parallel-HBHMC with AZCI method, (a) three-phase output voltages, output currents and two FBSM capacitor voltages of phase-*a*, (b) Output voltage of MHBC, corresponding voltage across WSC, phase-*a* current, and grid voltage.

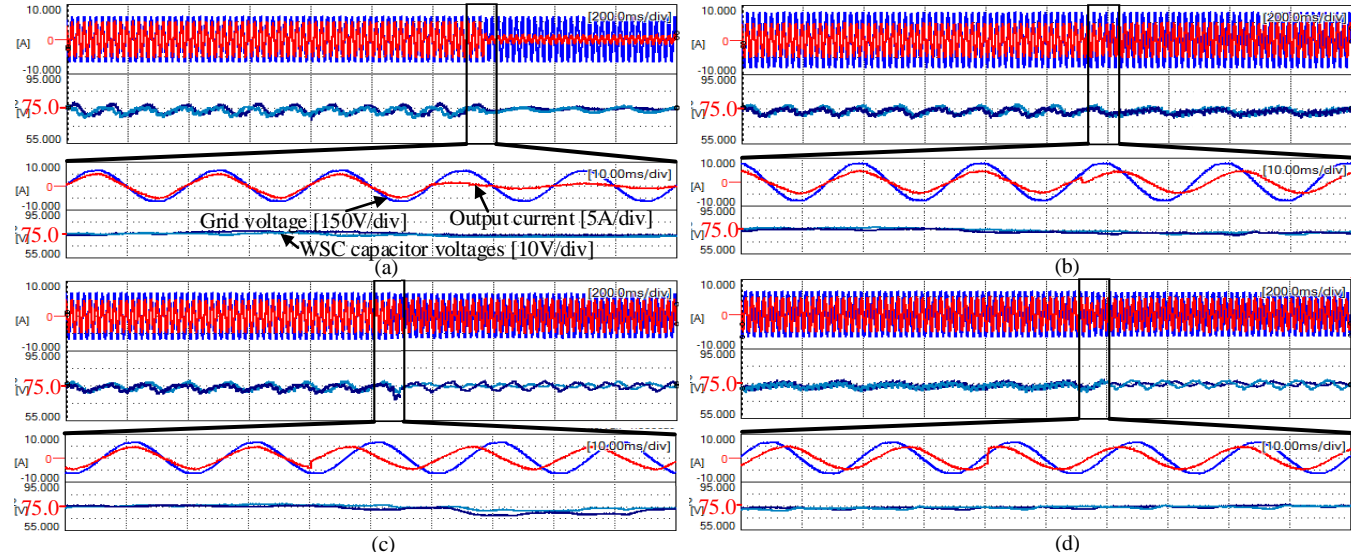


Fig. 23 Experimental waveforms of output current, grid voltage, and capacitor voltages of FBSM of WSC of series-HBHMC for (a) step change in current magnitude at unity power factor, (b) step change of current from unity to lagging power factor, (c) step change of current from unity to leading power factor, and (d) step change of current from lagging to leading power factor

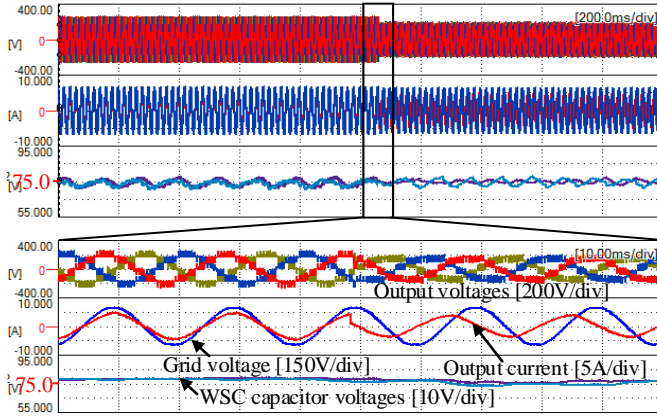


Fig. 24 Experimental results of three-phase output voltage, WSC capacitor voltages, output current and grid voltage for change of load current.

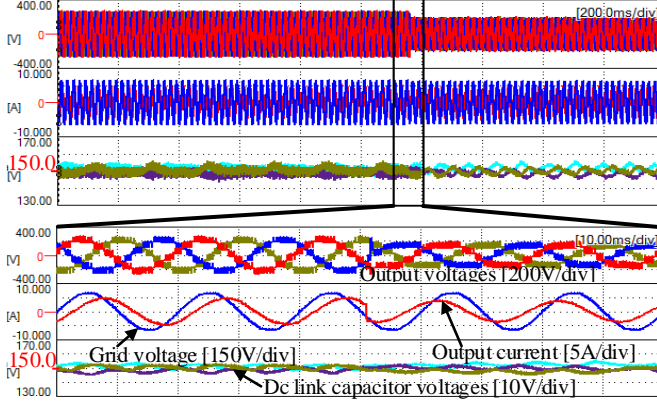


Fig. 25 Experimental results of three-phase output voltage, dc-link capacitor voltages, output current and grid voltage for change of load current.

It can be observed from Figs. 24 and 25 that the WSC and dc-link capacitors voltages remain well controlled irrespective of the mode and number of output voltage levels change. This further confirms satisfactory operation and effectiveness of the capacitor voltage control scheme for both overmodulation as well as undermodulation mode of HBHMC operation.

Fig. 26 demonstrates the converter performance when a dc pole-to-pole fault is created in the series-HBHMC prototype (Fig. 20). Before the fault occurrence the series-HBHMC is operated in inverting mode, supplying power to ac grid ($S1$ is closed and $S2$ is open (Fig. 20)). The dc fault is emulated by closing switch $S2$ and opening switch $S1$ and by inserting a resistance R in the fault current path to keep the fault current within safe limits. The gate pulses to the converter switches are blocked as soon as the fault is created. This causes the FBSMs capacitors to come in the path of the resulting current in the manner described above with reference to Fig. 15. Hence the ac currents quickly reduce to almost zero value. It can also be observed from Fig. 26 that since the fault current magnitude is negligibly small, the FBSMs capacitor voltages also do not experience any disturbance and effectively remain at their pre-fault values. The results in Fig. 26 reconfirm the effectiveness of the proposed converter in blocking dc side faults.

VI. LOSS EVALUATION

In this section, the loss evaluation studies of the HBHMC are carried out. For simplicity, the forward voltage drops of the insulated gate bipolar transistor (IGBT) and of the freewheeling diode are assumed to be identical and independent of the value of current flowing through them. This simplification

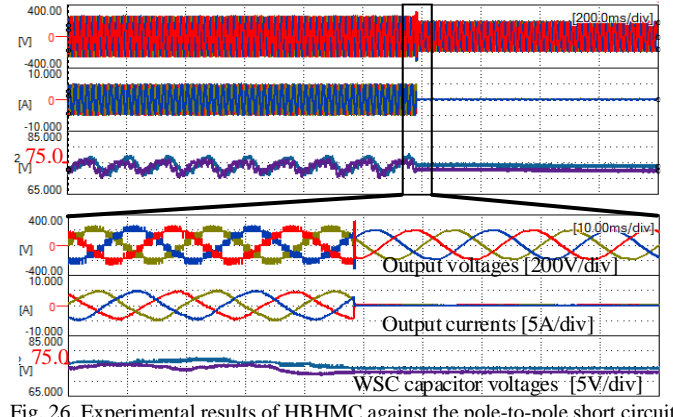


Fig. 26. Experimental results of HBHMC against the pole-to-pole short circuit: three-phase output voltage and current, and WSC capacitor voltages of phase-a

significantly reduces the calculation complexity [48]. Here the conduction loss is calculated as [48],

$$P_{cond} = \frac{1}{2\pi} \int_0^{2\pi} N V_{fd} |i_l| d(\omega t) . \quad (17)$$

where P_{cond} is the conduction loss of one phase-leg, N is the number of switches in the conduction path, V_{fd} is the forward voltage drop of the semiconductor switch, and i_l is the current flowing through the converter phase-leg. From (17), the total conduction losses for the HBHMC (P_{cHBHMC}) can be expressed as

$$P_{cHBHMC} = P_{cMHBC} + P_{cWSC} = \frac{1}{2\pi} \int_0^{2\pi} \left(N_{cMHBC} V_{fd} |I_x(t)| + N_{cWSC} V_{fd} |I_x(t)| \right) d(\omega t) \quad (18)$$

where P_{cMHBC} and P_{cWSC} are the conduction losses in the MHBC and WSC of HBHMC, respectively, and N_{cMHBC} and N_{cWSC} are the number of switches of MHBC and WSC in the conduction path, respectively.

The switching losses of each device are the sum of energy dissipation at each switching event, which are proportional to the current level. For convenience, the average current value is considered at each switching instant of each device. With this current the energy dissipation at the instant of turn-on and turn-off of each device is measured from the datasheet of the device. Moreover, for the antiparallel diode, the turn-on and turn-off energy dissipation is considered to be the same as that of IGBT switch. The number of switching events in one cycle multiplied with the energy dissipation at each such event yields the switching loss of each device [49]-[50], which is given by,

$$P_{swi} = f_{sw} (E_{on} + E_{off}) N_{sw} . \quad (19)$$

where P_{swi} is the switching loss of the converter, f_{sw} is the switching frequency, E_{on} and E_{off} are the energy dissipations at turn-on and turn-off of the device, respectively, and N_{sw} are the number of switching devices. E_{on} and E_{off} are obtained from the datasheet depending on the average value of current. As in (18), the total switching loss (P_{sHBHMC}) of the HBHMC is the sum of switching losses in MHBC and WSC and given as

$$P_{sHBHMC} = P_{sMHBC} + P_{sWSC} = \left(f_{sMHBC} (E_{on} + E_{off}) N_{sMHBC} + f_{sWSC} (E_{on} + E_{off}) N_{sWSC} \right) . \quad (20)$$

where P_{sMHBC} and P_{sWSC} are the switching losses in the MHBC and WSC of HBHMC, respectively, f_{sMHBC} and f_{sWSC} are the switching frequencies of the switches in MHBC and WSC of the HBHMC, respectively, and N_{sMHBC} and N_{sWSC} are the number of switching devices of MHBC and WSC, respectively.

Finally, the total loss of HBHMC can be estimated by sum of the conduction and switching losses and given as

$$P_{loss} = P_{chBHM} + P_{shBHM} \quad (21)$$

With the aforementioned assumptions the loss of HBHMC is calculated and compared with the MMC with HBSMs [1]-[4], [48] and MMC with FBSMs [20]. To have a fair and accurate loss comparison of the proposed HBHMC with the other converters, it is necessary to evaluate their losses for the same circuit parameters and devices. Hence, the same system is used for loss calculation of proposed HBHMC and other converter systems. As a loss calculation example, the system with 150 MVA at 0.8 power factor is considered. The other system specifications considered for the loss calculations are: dc-link voltage $V_{dcl} = 300$ kV, submodule capacitor voltage $V_c = 2.5$ kV. The Infineon (FZ1200R33KL2C) IGBT device characteristics is considered for the loss calculation [51]. Moreover, the following two different cases are considered for loss calculations:

- 1) The converters with equal ac side currents
- 2) The converters with equal ac power

At unity modulation index, the peak of output phase voltage of conventional MMC is $V_{dcl}/2$. However, the peak of output phase voltages of series-HBHMC and parallel-HBHMC are $V_{dcl}/3$ and V_{dcl} , respectively. As a result, in first case, the power delivered will be different for the topologies under consideration. In this case, the ac current magnitude of all the converters under consideration is considered same as that in the conventional MMC regardless of ac voltage magnitude. In second case, as the equal ac power is transferred from ac side to dc side, the series-HBHMC has to carry higher current (1.5 times) and parallel-HBHMC has to carry lower current (0.5 times) than the conventional MMC phase current. Nevertheless, for the same dc-link voltage, the required number of semiconductor devices are lesser for series-HBHMC and higher for parallel-HBHMC than the conventional MMC. The conduction losses, switching losses and total losses of the different converters are shown in Fig. 27.

It can be observed from Fig. 27 that the losses of the proposed series-HBHMC topology, in case of the same ac power, are greater than those of the MMC with HBSMs but less than those of the MMC with FBSMs. However, as compared to MMC with HBSMs, the series-HBHMC has some additional features like dc fault tolerant capability, small footprint structure, high dc-link utilization, and an extra degree of freedom for SM capacitor voltage balancing. On the other hand, the parallel-HBHMC has lower losses as compared to MMC with HBSMs. This is because only half of the ac current is required to transfer same ac power as compared to MMC with HBSMs. However, the number of SMs are higher in case of parallel-HBHMC.

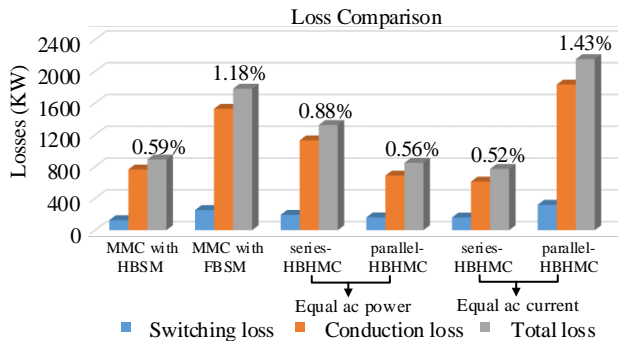


Fig. 27. Conduction, switching and total losses of MMC with HBSM [1]-[4], [48], MMC with FBSM [20], and proposed HBHMC.

Moreover, the series-HBHMC losses are lower and parallel-HBHMC losses are higher than the losses of MMC with HBSMs and MMC with FBSMs in case of the same ac current. The detailed comparison of the proposed HBHMC topology with the other major VSC HVDC converter topologies in terms of the required number of semiconductor devices is given in the next section.

VII. COMPARISON OF HBHMC WITH EXISTING TOPOLOGIES

A comparison of the proposed HBHMC topology with the other major VSC HVDC converter topologies is carried out in terms of the required number of semiconductor devices and capacitors for the same dc-link voltage. The MMC topology with HBSMs is considered as the benchmark topology for this comparison study. For comparison $N = V_{dcl}/V_{sw}$ is defined, where V_{sw} is the rated voltage of one SM, V_{dcl} is the total dc-link voltage and N represents the total SM count required in each arm of MMC. Moreover, for comparing the possible number of converter output voltage levels, the non-interleaved modulation technique is considered for MMC [44]. The number of possible output voltage levels for all topologies is determined for the modulation index of one.

Table VI summarizes the comparison of the proposed series-HBHMC and parallel-HBHMC topologies with the other major HVDC converter topologies, such as, MMC with HBSMs [1]-[4], MMC with all FBSMs [20], Hybrid MMC (50% HBSMs and 50% FBSMs) [22], HCMC [23]-[26], AAMMC [27]-[29], parallel hybrid MMC [33], [34], and CTFB-HMC [35]. It is clear from Table VI that numbers of switches and capacitors required for the series-HBHMC are very less as compared to those in the other topologies. Moreover, the number of switches in the conduction path for the series-HBHMC is lesser than all the other converter topologies. Also, since the MHBC of the proposed configuration operates at the fundamental frequency, the series-HBHMC is expected to have lower losses. However, for the same dc-link voltage in all topologies, the maximum ac output voltage obtained from the series-HBHMC is lower, which increases the current rating requirement of converter switches for the same power. The parallel-HBHMC although requires more number of devices for the same dc-link voltage, but it offers high utilization of the dc bus. Hence the series-HBHMC topology can be more suitable for the applications with very high dc-link voltage and lower current requirements, while the parallel-HBHMC can be more suitable for the applications with lower dc-link voltage and higher current requirements.

It is also to be noted that in contrast to the MMC, the modularity is limited in HBHMC as far as the MHBC part of the converter is concerned. Nonetheless, the WSC part of the converter does offer modularity. It also has a lot of additional advantages over MMC, like; dc fault tolerant capability, small footprint structure, high dc-link utilization, an extra degree of freedom for SM capacitor voltage balancing and as explained earlier in Sec. II, this topology can also be extended to high voltage-low current (series-HBHMC) or low voltage-high current (parallel-HBHMC) applications. However, in contrast to MMC where an interfacing transformer for grid connection may be avoided [2], the proposed HBHMC topology would require an interfacing transformer for all three-phase applications. Moreover, in contrast to the HCMC topology, the proposed HBHMC uses symmetrical modulation technique and

TABLE VI
COMPARISON OF THE HBHMC WITH EXISTING TOPOLOGIESs

	MMC with HBSMs [1]-[4]	MMC with FBSMs [20]	MMC (50% HBSMs and 50% FBSMs) [22]	Hybrid Modular converter [23]-[26]	AAMMC [27]-[29]	Parallel Hybrid MMC [33] [34]	CTFB- HMC [35]	Series- HBHMC	Parallel- HBHMC
dc voltage	V_{dct}	V_{dct}	V_{dct}	V_{dct}	V_{dct}	V_{dct}	V_{dct}	V_{dct}	V_{dct}
Max ac voltage	$V_{dct}/2$	$V_{dct}/2$	$V_{dct}/2$	$V_{dct}/2$	$V_{dct}/2$	$V_{dct}/2$	V_{dct}	$V_{dct}/3$	V_{dct}
Output voltage levels	N+1	N+1	N+1	N+1	N+1	N+1	2 N + 1	(2N/3)+1	2 N + 1
No. of switches (3 phase)	12N	24N	18N	12N	15N	9N	24N	8N	24N
No. of switches in conduction path	6N	12N	9N	6N	4.5N	4.5N	6N	4N	12N
No. of capacitors (3 phase)	6N	6N	6N	1.5N	3N	1.5N	3N	N	3N
Voltage stress of switches	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N	V_{dct}/N
Soft switching of DSs	NA	NA	NA	No	Yes	Yes	No	No	No
dc Fault tolerant	No	Yes	Yes	Yes	Yes	No	No	Yes	Yes
Overmodulation	No	Yes	Yes	Yes	Yes	No	No	Yes	Yes

the switches of MHBC operate at the fundamental frequency [24], [25]. Also, for the voltage control of WSC in HBHMC no third harmonic injection is required. The HBHMC utilizes full dc-link voltage for output voltage generation as opposed to HCMC, which uses only half of the dc-link voltage [24], [25], [31]. It is also to be noted that the parallel-hybrid topology does not have a dc fault tolerant capability and it would require third-harmonic injection and additional submodules for operating in the overmodulation region [33].

Hence, it is clear from above that the HBHMC topology is a promising candidate for the HVDC applications.

VIII. CONCLUSION

This paper proposes an H-bridge hybrid multilevel converter topology, HBHMC, for HVDC applications. The proposed converter is a dc fault tolerant hybrid topology, which uses cascaded FBSMs (i.e. WSC) connected to the output of the MHBC. The WSC helps in generating the multilevel voltage waveform at the HBHMC output. For a three-phase circuit, three such HBHMCs can be connected in series on the dc side to handle a high dc-link voltage. Similarly, they can instead be connected in parallel across the dc-link for high dc current. In this paper, the basic operation of HBHMC and new modulation techniques to balance the capacitor voltages of HBHMC by appropriately selecting an operating mode (isolation mode: HCI and AZCI methods) are presented. The suggested voltage control methods are simple and easy to implement. Moreover, both the HCI and the AZCI methods are designed in a way that the MHBC always operates at the fundamental frequency to reduce the switching losses of converter. Further, the AZCI method offers more advantages than the HCI method, such as, smaller value of submodules capacitance and ability to operate in the overmodulation mode. Some of the other prominent advantages of the proposed converter are: (i) extra degree of freedom for capacitor voltage balancing, (ii) fewer semiconductor devices and capacitors in series-HBHMC, (iii) higher dc-link utilization in parallel-HBHMC, and (iv) inherent dc fault current blocking capability. Simulation and experimental studies are performed to validate the proposed converter topology and capacitor voltage control methods.

The effectiveness of proposed HBHMC and its control strategies for HBHMC-based HVDC system are investigated using PSCAD/EMTDC simulations under various operating conditions. The simulation studies show that the HBHMC has good performance under normal, dc fault, and grid voltage unbalance conditions. Moreover, the effectiveness of proposed

converter is verified experimentally by using a three-phase grid connected HBHMC porotype. The obtained experimental results demonstrated that the proposed control method is effective in controlling WSC capacitor voltages under different operating conditions. It is also demonstrated that the HBHMC provides the desired dc fault tolerant capability.

The simulation and experimental results highlight excellent performance of the proposed converter topology and control schemes. Hence, the HBHMC can be a good alternative for HVDC applications where dc fault blocking capability is required.

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